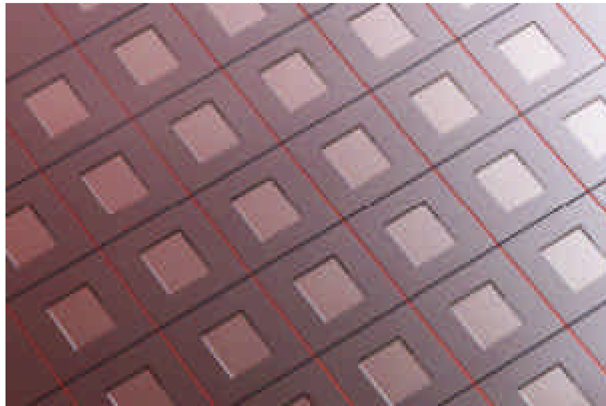
MEMS: Mainstream Process Integration

Introduction: A Counter-Revolution in MEMS Technology

The picture below shows a prototype example of foundry-based, wafer scale, hermetic encapsulation for optical MEMS arrays. The resulting wafer is fully compatible with conventional back-end processing. For the first time, MEMS can leverage mainstream technologies for dicing, packaging and assembly – a breakthrough that will revolutionize the cost and range of application of MEMS.

MEMS: Founded on Technology Leverage

MEMS technology quickly transitioned from innovative concepts to practical demonstrations and on to early products . The speed of this transition was entirely based on an ability to leverage the manufacturing base of the integrated circuit (IC) industry: plant, equipment, tooling, processes, materials, and people. Virtually the entire infrastructure of a $100B industry could be co-opted to support MEMS technology (Chin, 2001; MEMS Exchange).



If the initial success of MEMS technology was based on similarity to the IC industry, current problems limiting the growth of MEMS markets are rooted in fundamental differences between MEMS and IC's (O'Neal, 1999; Romig & Smith, 1997). This has kept MEMS out of the mainstream.

Ziptronix is positioned to solve these problems and greatly improve MEMS leverage of the IC industry, driving rapid expansion of MEMS markets.

The Crucial Differences Between MEMS and ICs

1. ICs are essentially flat. MEMS are typically not.

2. ICs depend on effects buried beneath the surface of the IC. MEMS are essentially surface-effect devices.

3. ICs have no moving parts. MEMS typically move.

4. ICs are built in a way that makes them insensitive to their environment before they exit the carefully controlled world of the IC foundry in wafer form. MEMS in wafer form are typically extremely sensitive to their environment until they are packaged. This sensitivity makes every post-foundry MEMS handling step (wafer dicing, placement in a package, formation of electrical connections, package closure) different from IC handling (nonstandard), and very expensive.

The Opportunity

These differences provide an enormous opportunity to create value. Consider the following:

- The critical benefit from ICs is integration! The first PC processor had fewer than 30,000 transistors; today processors integrate more than 100,000,000 transistors. This ability to integrate increasing functionality is the heart of the value proposition of electronics – the heart of the celebrated "Moore's Law," which states

that *"…functionality doubles every 18 months and costs remain flat."* Relatively speaking, MEMS devices are not benefiting from this level of accelerated integration. While it is common for an IC to combine memory, computation, and communication, MEMS devices typically perform a single function and must be combined with other devices (usually IC's) to create a useful product. This limitation is rooted in the MEMS process flow (manufacturing recipe), which is significantly different from the flow used to build IC's (Ramesham & Ghaffarian, 2000). Combination flows that might build both MEMS capabilities and IC functionality on the same chip suffer from classic "least common denominator" tradeoffs – compromised IC performance, compromised MEMS performance, and high cost. The cost outlook is particularly bleak. IC processes are often measured in mask levels. A typical process may have 30 mask levels. The SIA industry roadmap section on SOC estimates that modifications to the IC process to support an embedded MEMS solution could add as many as 14 mask levels. Such an increase in process complexity along with the required increase in die area for the MEMS function would severely impact yield and cost. (Yield has an inverse exponential dependence on die area and process complexity.)

Cost effective integration of MEMS with ICs creates value

- Because MEMS devices are on the wafer surface and move, they often require a free surface (headspace).. As a result, at the end of wafer processing, when the devices are separated (usually by sawing the wafer) and packaged, MEMS devices cannot be handled like IC's (O'Neal et al., 1999). Each individual chip (die) requires special handling and special packaging (Romig & Smith, 1997), which creates a huge cost disadvantage. As a result, while IC's have well-developed standards and infrastructure for these operations, MEMS packaging is largely custom and represents a much higher fraction of the cost of goods than does packaging of IC's (40 to 90% of cost) (Bratter, 2000; O'Neal et al., 1999; Reichl & Grosser, 2001).

Foundry-based, Wafer Scale MEMS Encapsulation creates value

- To first order, MEMS devices exploit the mechanical properties of materials, while ICs exploit electronic properties. Thus mechanical perturbations are a first order effect for MEMS, and a second order effect for ICs.. As a result, packaging strategies that are proven reliable for ICs often severely compromise MEMS performance. This is particularly true of stress (the application of a force to a material) (O'Neal et al., 1999). For example, epoxy may be used to "glue" an IC into a package. If the same materials and methods are used to "glue" a MEMS device to a package, the performance and reliability of the device may be significantly changed. Moreover, stress effects can vary with normal changes in operating temperature. Uncontrolled, this often results in unacceptable variations in device performance. At the same time, controlled stress can be used to enhance device performance or stability.

Chemistry Compatibility in MEMS Encapsulation creates value

- As discussed above, an encapsulated MEMS device often requires surface clearance or "headspace". At the same time, device reliability may require rigorous control of headspace chemistry. Various treatments ranging from simple desiccants to "lubricity enhancing agents" or other proprietary treatments can be crucial. Surface treatments can be unintentionally altered during encapsulation or during device operation by outgassing of seal materials or permeation effects that compromise hermeticity (O'Neal et al., 1999; Ramesham & Ghaffarian, 2000).

The Ziptronix Solution

Ziptronix technology achieves the following:

- Enables a MEMS die to be handled conventionally and integrated with other system components;

- Encapsulates MEMS at wafer scale in the MEMS foundry, greatly reducing the expense of post-foundry operations and establishing a basis for standardized packaging;

- Uses room temperature processing and a broad selection of material choices to establish a versatile basis for stress engineering, ranging from simple stress minimization to materials integration for temperature compensation, or other performance enhancements;

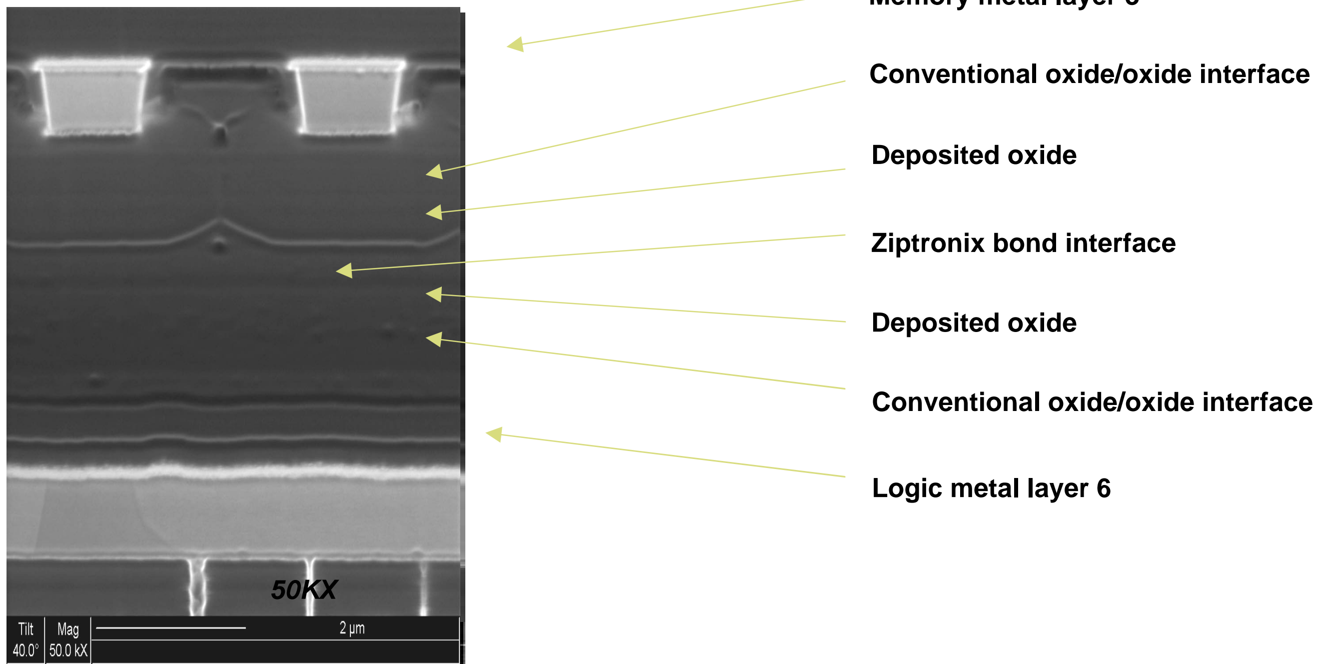
- Eliminates epoxies or other materials that require curing, and instead uses established IC processing materials such as SiO_2 to create a true hermetic seal. These process features, along with MEMS-specific variations in surface activation, allow us to establish and maintain a variety of proprietary headspace chemistries.

In short, Ziptronix creates value by providing solutions for the key problems limiting the growth of MEMS markets today. Ziptronix will bring these answers to market quickly by directly leveraging tooling, materials, and process chemicals used throughout the IC industry.

Ziptronix: Room Temperature, Adhesive-less Bonding Technology

Room Temperature Covalent Bonding: Ziptronix' proprietary ZiROC™ technology creates room temperature, covalent bonding between the surfaces of materials commonly used in ICs. Materials that are typically bonded include: SiO_2 (in various forms), Si, and Si_3N_4 (Process variations for other materials, such as diamond-like carbon, DLC, are under development). Note that GaAs or other exotic materials may be coated with SiO_2 and bonded to a Si IC. From a bonding perspective this is a SiO_2 to SiO_2 bond. This approach creates a huge menu of integration choices.

The following micrograph is an image of the cross section of a Ziptronix bonded structure. The image is formed using secondary electron microscopy (SEM). In such an image "features" are due to variations in electron escape from the surface. Unlike normal light-based images, these electron-based images are sensitive to variations in chemistry and bonding. The image shown contains several conventional oxide/oxide interfaces. These were formed by industry standard oxide deposition processes in which an oxide layer is deposited on an identical, existing oxide layer, and the resultant interfaces are easily seen. In contrast, the bonding interface created with ZiROC™ technology is not visible. This indicates chemical and structural homogeneity through the bonded interface. In short, ZiROC™ bonding at the interface is equivalent to the bonding in the bulk oxide materials.



Materials to be bonded are processed by chemo-mechanical polishing, CMP, to establish a planar surface where the bond is to be formed. For convex MEMS applications (where the MEMS structure extends above the surface of the wafer), this planarization step typically occurs early in the fabrication flow of the MEMS wafer. The cap wafer is similarly planarized. The fraction of the surface required for bonding is very small. – a narrow rim (<200 microns) around the device will suffice. Relief structures are routinely included in the cap wafer to achieve headspace.

Prior to bonding, a proprietary process is used to activate one or both of the surfaces to be bonded. Single-sided versus double-sided activation may be used to accommodate proprietary headspace chemistries. Following activation, the surfaces bond covalently on contact at room temperature. Bonding is carried out in normal foundry ambient—a vacuum or inert gas environment is not required. No applied pressure or electric field is used, the surfaces are simply brought into contact. For wafer to wafer bonding at 8" wafer scale, the bond forms within seconds. For die to wafer applications, the bond is essentially instantaneous, enabling compatibility with conventional high-speed pick and place.

Room temperature bonding has multiple advantages:

- No thermal degradation of sensitive components;
- No unintentional built-in stress resulting from differences in coefficient of thermal expansion of the components to be bonded;
- No pattern/stress distortion ("pincushioning") due to limited area bonding at different temperatures as the wafer pair is ramped to the "bonding" temperature;
- Conventional tooling is used for wafer and die alignment and bonding, greatly reducing equipment and tooling costs;
- Throughput is limited by the mechanism of the tool, not the requirements of the process, resulting in much higher throughput;

- The process runs today at 200 mm wafer scale and readily extends to 300 mm.

Hermeticity: Practical Considerations

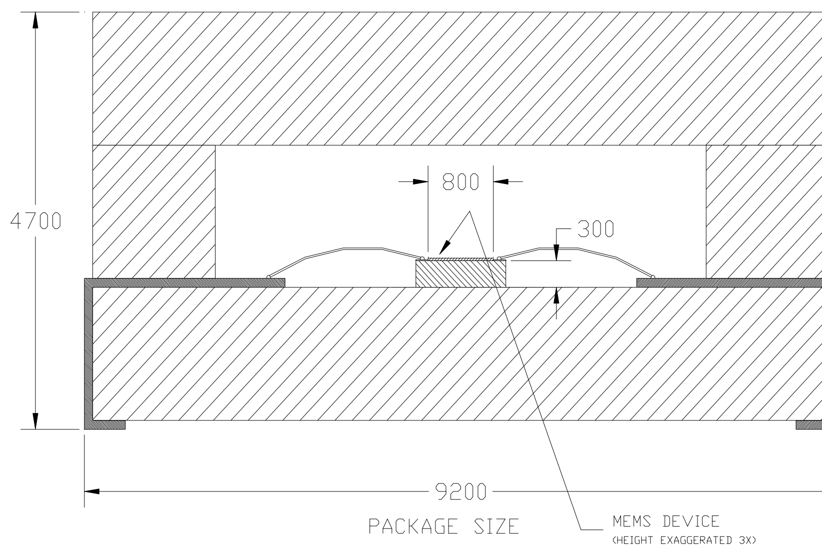
The initial yield and service reliability of MEMS devices depends on controlling the device environment. At a minimum, when encapsulated there must be no exchange with the external environment (leakage). Several other factors are equally important:

- "Outgassing" or evolution of species in solid solution in the materials used to form the headspace enclosure;
- Permeation (diffusion) of external species through enclosure materials, such as water vapor through epoxy;
- Control of the manufacturing environment prior to "sealing" of the device.

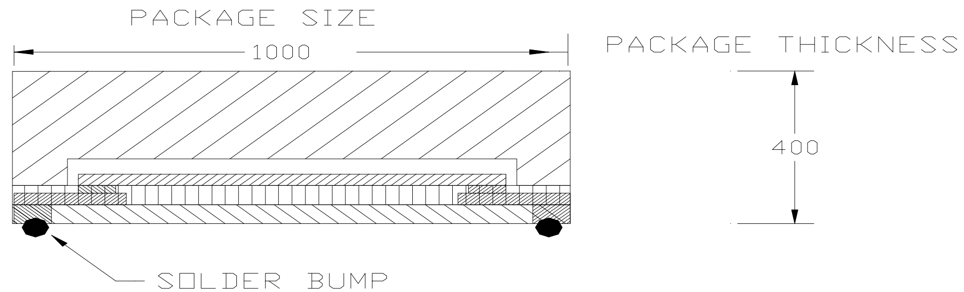
These factors are best controlled by:

1. **Strictly limiting the list of materials used.** Ziptronix's ZiROC™technology uses only materials that are normally part of the MEMS structure itself (Si and SiO_2 may be used for encapsulation).

2. **Creating the minimum surface area internal to the headspace volume**. As shown below, conventional soldered ceramic packages must accommodate internal wirebonds, die attach materials, etc. resulting in a package volume many times larger than the die volume.

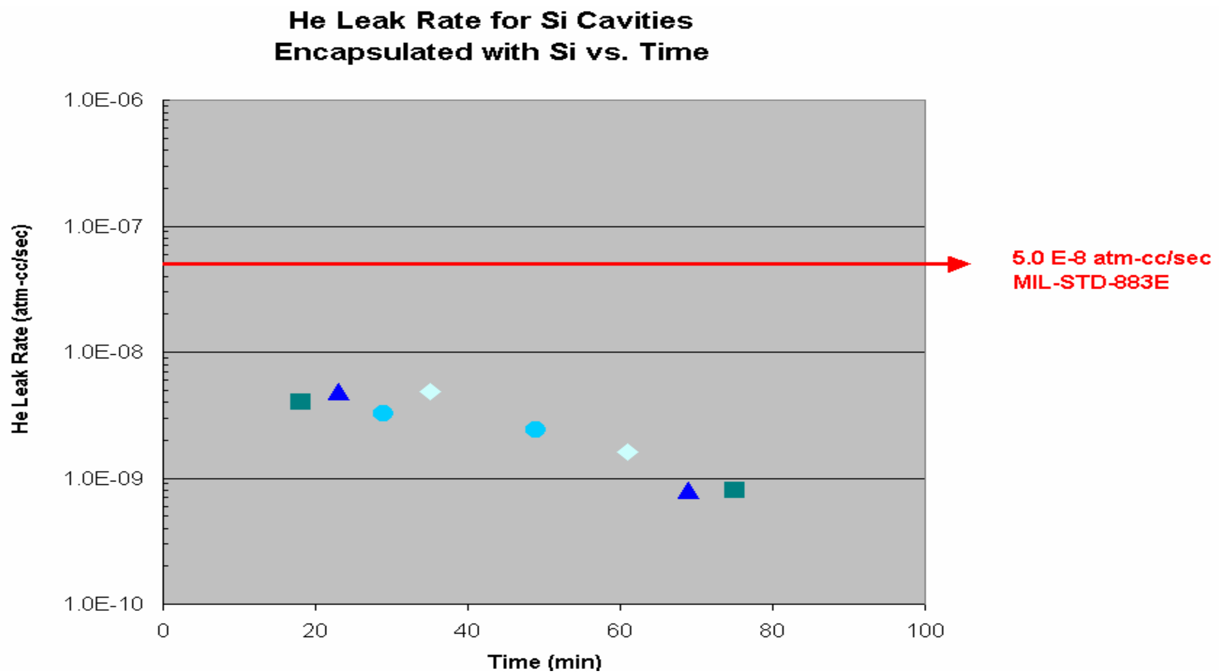


The Ziptronix approach encapsulates only the active MEMS device -- wirebonds or ball grid attach volumes and associated materials are external to the hermetic MEMS volume. The configuration shown below provides full hermeticity in a chip scale package, creating huge savings in footprint and volume.



3. **Achieving hermeticity early in the product flow**. Ziptronix creates hermeticity as a wafer scale operation at the end of the MEMS foundry flow – before any dicing, packaging or assembly operations. This significantly increases yield and reduces post-foundry unit process costs.

Hermeticity data for MEMS cavities fabricated using ZiROC™ technology are shown below. Note the results are an order of magnitude better than the MIL-STD-883E standard. ZiROC™ has also successfully passed accelerated life (pressure and temperature cycle) testing to automotive reliability specifications.



Electrical Connections: A Range of Options

MEMS devices have traditionally been wirebonded inside of a ceramic cavity, and for many applications wirebonding will remain important. Ziptronix provides wirebonding options at chip scale, where the wirebonds are external to the hermetic cavity. Increasingly, footprint and volume constraints as well as impedance issues for high frequency products – such as cellular handsets – demand bump bonding configurations. Ziptronix provides a range of chipscale bumping options.

Summary:

Ziptronix technology allows MEMS devices to exit the fabrication facility as passivated wafers that are fully compatible with conventional back-end processing. This creates enormous leverage and opportunities for cost reduction. For the first time, MEMS die can now be handled like a conventional IC, which is critical if MEMS are to be included in mainstream packaging and assembly trends.

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